

# INTEGRATED CIRCUITS LIST OF COMPARABLE TYPES T T L RANGE

## COMMERCIAL VERSIONS

<i>Type No.</i>	<i>Mullard types</i>	<i>Type No.</i>	<i>Mullard types</i>
7400N	FJH131	7454N	FJH181
7401N	FJH231	7460N	FJY101
7401AN	FJH311	7470N	FJJ101
7402N	FJH221	7472N	FJJ111
7403N	FJH291	7473N	FJJ121
7403AN	FJH301	7474N	FJJ131
7404N	FJH241	7475N	FJJ181
7405N	FJH251	7476N	FJJ191
7405AN	FJH321	7480N	FJH191
7410N	FJH121	7482N	FJH201
7420N	FJH111	7490N	FJJ141
7430N	FJH101	7491AN	FJJ151
7440N	FJH141	7492N	FJJ251
7441AN	FJL101	7493N	FJJ211
7442N	FJH261	7496N	FJJ241
7450N	FJH151	74107N	FJJ261
7451N	FJH161	74121N	FJK101
7453N	FJH171		
<i>Type No.</i>	<i>Mullard types</i>	<i>Type No.</i>	<i>Mullard types</i>
6400N	FJH136	6453N	FJH176
6410N	FJH126	6454N	FJH186
6420N	FJH116	6460N	FJY106
6430N	FJH106	6470N	FJJ106
6440N	FJH146	6472N	FJJ116
6450N	FJH156	6473N	FJJ126
6451N	FJH166	6474N	FJJ136
		6476N	FJJ196

There is also a limited range of devices available in the '2' series (extended temperature range —55 to +125°C).

# T.T.L. DUAL MASTER-SLAVE JK FLIP-FLOPS WITH PRESET AND CLEAR

**FJJ191**  
**FJJ191A**  
**FJJ196**

Correspond to 74 Series types 7476N, 6476N

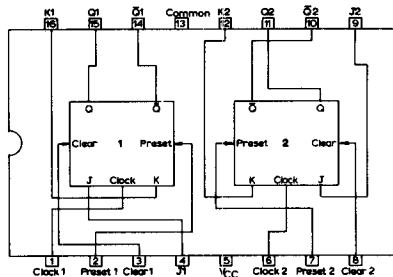
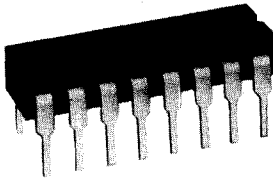
## TENTATIVE DATA

These devices are transistor-transistor logic dual JK master-slave flip-flops, with preset and clear inputs, in the FJ series of integrated circuits. The FJJ191 corresponds to '74 Series' type 7476N, the FJJ196 corresponds to '64 Series' type 6476N.

QUICK REFERENCE DATA		
Supply voltage (nominal)	5.0	V
Max. clock rate	10	MHz
Fan-out (each output)	10	
Noise immunity (typ.)	1.0	V
(min.)	0.4	V
Average power dissipation (per flip-flop) (50% duty cycle, $T_{amb} = 25^{\circ}C$ )	40	mW

OUTLINE (see page 6)

- FJJ191 - 16-lead all plastic dual-in-line package
- FJJ191A - 16-lead hermetic-in-plastic dual-in-line package
- FJJ196 - 16-lead all plastic dual-in-line package



## LOGIC FUNCTION

Dual master-slave JK flip-flop with single J and K inputs. 'Low' input to preset sets Q to logical '1' regardless of clock state. 'Low' input to clear sets Q to logical '0' regardless of clock state.

DESIGN DATA (Maximum adverse operating conditions assumed)

		Min.	Nom.	Max.	
<b>Temperature</b>					
Operating ambient	FJJ191/1A	0	-	70	°C
	FJJ196	-40	-	85	°C
<b>Supply</b>					
Supply voltage	FJJ191/1A	4.75	-	5.25	V
	FJJ196	4.5	-	5.5	V
Supply current (per flip-flop)		-	8.0	-	mA
<b>Inputs</b>					
Voltage for 'High' input state	S.N.I. = 0	2.0	-	-	V
	S.N.I. = 0.4V	2.4	-	-	V
<b>*Current for 'High' input state</b>					
J and K inputs		-	-	40	μA
Preset and Clear inputs		-	-	80	μA
Voltage for 'Low' input state	S.N.I. = 0	-	-	0.8	V
	S.N.I. = 0.4V	-	-	0.4	V
<b>**Current for 'Low' input state</b>					
J and K inputs		-	-	1.6	mA
Preset, Clear and Clock inputs		-	-	3.2	mA
<b>Outputs</b>					
Voltage for 'High' output state		2.4	-	-	V
Voltage for 'Low' output state		-	-	0.4	V
Output resistance in 'High' output state		-	100	-	Ω
Output resistance in 'Low' output state		-	12	-	Ω
Current capability at 'Low' output state		-	-	16	mA
<b>Fan-out</b>					
J and K inputs		-	-	10	
Preset, Clear and Clock inputs		-	-	5	
Maximum clock rate		10	15	-	MHz
Clock pulse width		20	-	-	ns
<b>Performance</b>					
Signal noise immunity		0.4	1.0	-	V
Average propagation delay time ( $C_L = 15\text{pF}$ )		-	30	-	ns
This is equivalent to a propagation delay time to the 'Low' state of 34ns and to the 'High' state of 26ns.					
*The 'High' state normally corresponds to a voltage level between 2.4 and 5.25V.					
**The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.					



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**FJJ191  
FJJ191A  
FJJ196**

DESIGN DATA (cont'd)

Truth table (abbreviated)

$t_n$		$t_{n+1}$ Q
J	K	
Low	Low	$Q_n$
Low	High	Low
High	Low	High
High	High	$\overline{Q}_n$

Notes

1.  $t_n$  = bit time before trailing edge of clock pulse
2.  $t_{n+1}$  = bit time after clock pulse
3. Clear and Clock inputs operate on negative going signals

## CHARACTERISTICS

$T_{amb} = 25^\circ\text{C}$ , Supply voltage = 5.0V

Bistable must be set with Q to '0' prior to making these tests

		Min.	Typ.	Max.
$V_{TH}$	'Low' Input threshold voltage for 'Low' input state (Preset or Clear inputs) ( $I_{out} = -400\mu\text{A}$ , $V_{out}(Q \text{ or } \overline{Q}) = 2.4\text{V}$ , $V_{clock}$ and $K = 2.0\text{V}$ )	0.8*	-	- V
$V_{TH}$	'High' Input threshold voltage for 'High' input state (Preset or Clear inputs) ( $I_{out} = 16\text{mA}$ , $V_{out}(Q \text{ or } \overline{Q}) = 0.4\text{V}$ , $J = K = \text{Clock} = 2\text{V}$ )	-	-	2.0* V
$V_{out}$	'Low' ‡Output voltage for 'Low' output state (Preset or Clear inputs) ( $I_{out} = 16\text{mA}$ , $J = K = \text{Clock} = 2\text{V}$ , $V_{preset} = 2\text{V}$ , $V_{clear} = 0.8\text{V}$ )	-	-	0.4* V
$V_{out}$	'High' ‡Output voltage for 'High' output state (Preset or Clear inputs) ( $I_{out} = -400\mu\text{A}$ , $J = K = \text{Clock} = 2\text{V}$ , $V_{preset} = 0.8\text{V}$ , $V_{clear} = 2\text{V}$ )	2.4*	-	- V



CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.
$I_{in}$ 'Low'	J or K current for 'Low' input state ( $V_{in}=0.4V$ , $V_{clear}=V_{clock}=4.5V$ )	-	-	1.6* mA
$I_{in}$ 'Low'	†Preset, Clear or Clock input current for 'Low' input state ( $V_{in}=0.4V$ , $J=K=4.5V$ )	-	-	3.2* mA
$I_{in}$ 'High'	Preset or Clear input current for 'High' input state ( $V_{in}=2.4V$ , $V_{clock}=0$ )	-	-	80* $\mu A$
$I_{in}$ 'High'	J or K input current for 'High' input state ( $V_{in}=2.4V$ , $V_{clock}=0$ )	-	-	40* $\mu A$
$I_{out}$ s/c 'High'	‡Short circuit output current for 'High' output state ( $V_{clock}=0$ , $J=K=4.5V$ , $V_{preset}=0$ , output Q grounded)	18*	-	57* mA

\*These are the characteristics which are recommended for acceptance testing purposes.

†The  $\bar{Q}$  output or Clear input is momentarily grounded to achieve correct output state before commencing measurement.

‡The conditions stated refer to the measurement of Q. To measure  $\bar{Q}$  the conditions are:-

for $V_{out}$ 'Low'	$V_{preset} = 0.8V$ , $V_{clear} = 2.0V$
for $V_{out}$ 'High'	$V_{preset} = 2.0V$ , $V_{clear} = 0.8V$
for $I_{out}$ s/c 'High'	replace $V_{preset}$ by $V_{clear}$

Switching characteristics ( $C_L = 15pF$ , Fan-out = 10)

		Min.	Typ.	Max.
	Set up time	20	-	- ns
	Hold time	0	-	- ns
	Clock frequency	10	15	- MHz
	Clock pulse width	20	-	- ns
	Preset and clear pulse width	25	-	- ns
$t_{pd0}$	Propagation delay time to logical '0' level from Clock to output	10	-	50 ns
$t_{pd1}$	Propagation delay time to logical '1' level from Clock to output	10	-	50 ns
$t_{pd0}$	Propagation delay time to logical '0' level from Preset or Clear to output	-	-	50 ns
$t_{pd1}$	Propagation delay time to logical '1' level from Preset or Clear to output	-	-	50 ns



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**FJJ191  
FJJ191A  
FJJ196**

## CHARACTERISTICS (cont'd)

### Switching characteristics

Note:-  $C_L$  = Total capacitance of driven gates including wiring capacitance.

Switching waveforms - See separate sheet

### RATINGS

Limiting values of operation according to the absolute maximum system.

#### Electrical (pin 13 earthed)

Maximum positive supply voltage (pin 5)	7.0	V
Maximum continuous input voltage (pins 1, 2, 3, 4, 6, 7, 8, 9, 12, 16)	5.5	V
Maximum negative transient input voltage ( $t_p = 20\text{ns}$ , $f = 5.0\text{MHz}$ , $R_s \geq 75\Omega$ )	-2.0	V
Minimum width of clock pulse	20	ns
Minimum width of preset or clear pulse	25	ns

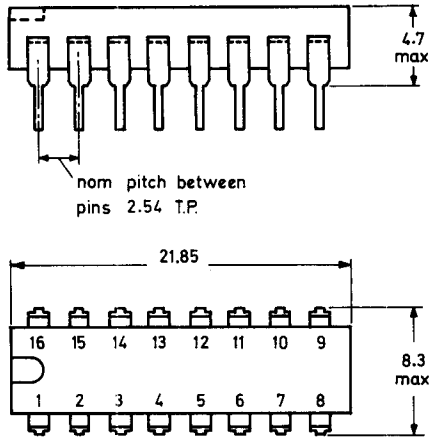
#### Temperature

$T_{stg}$ min.		-65	$^{\circ}\text{C}$
$T_{stg}$ max.		150	$^{\circ}\text{C}$
$T_{amb}$ operating range	FJJ191/1A	0 to +70	$^{\circ}\text{C}$
$T_{amb}$ operating range	FJJ196	-40 to +85	$^{\circ}\text{C}$



# OUTLINE AND DIMENSIONS

16-lead dual-in-line package



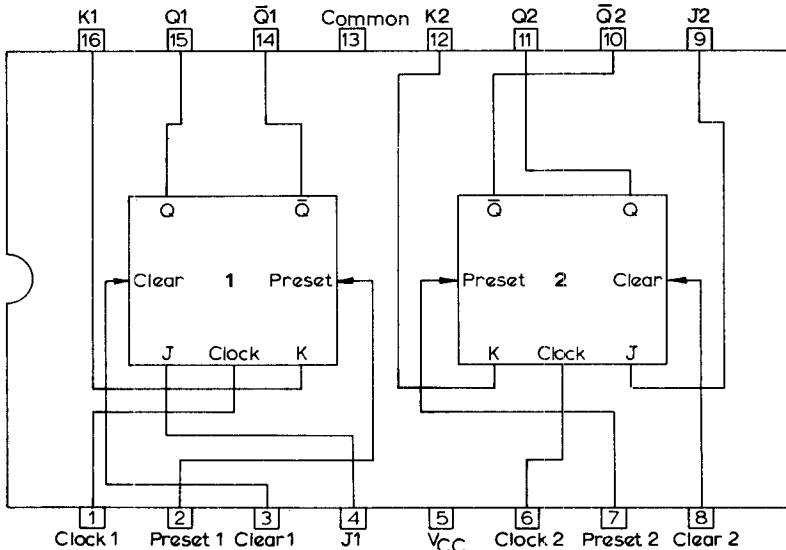
## PINNING

1. Clock input 1
2. Preset input 1
3. Clear input 1
4. J input 1
5. Supply voltage
6. Clock input 2
7. Preset input 2
8. Clear input 2
9. J input 2
10.  $\bar{Q}$  output 2
11. Q output 2
12. K input 2
13. Common
14.  $\bar{Q}$  output 1
15. Q output 1
16. K input 1

For detailed dimensions see General Explanatory Notes

For Handling Notes see General Explanatory Notes

## LOGIC DIAGRAM



Positive logic

'Low' input to Preset sets Q to logical '1'

'Low' input to Clear sets Q to logical '0'

